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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,418	07/21/2003	Narumi Ohkawa	030882	4101
38834 7590 10/05/2007 WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036			EXAMINER TRAN, NHAN T	
			ART UNIT 2622	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/623,418

Applicant(s)

OHKAWA, NARUMI

Examiner

Nhan T. Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 6-40 is/are pending in the application.
- 4a) Of the above claim(s) 3, 4, 6-27, 29-32, 34, 35, 37 and 38 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 40 is/are allowed.
- 6) ☒ Claim(s) 1, 28, 33, 36 and 39 is/are rejected.
- 7) ☒ Claim(s) 2 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 7/5/2007 have been fully considered but they are not persuasive.

The Applicant argues that Koizumi does not teach that the photoelectric converters and the amplifying transistors of all the rows are simultaneously reset, and charges transferred from the photoelectric converters to the amplifying transistors of all the rows are simultaneously performed.

In response, the Examiner respectfully submits another embodiment of Figs. 18-20 of Koizumi that teaches above-mentioned feature as will be discussed in details in the rejection section 5 below.

The Applicant also argues that Koizumi in view of Guidash fails to teach the limitations of previous claim 5, which is now incorporated into claim 1, that includes photoelectric converter and the first transistor being adjacent to each other in the row direction, the second transistor and the third transistor being adjacent to each other in the column direction, the gate electrode of the first transistor and the gate electrode of the fourth transistor being extended in the column direction.

In response, the Examiner respectfully disagrees. The above-mentioned layout features of claim 1 are taught by Guidash as further discussed in the rejection section 6 below.

Claim Objections

2. Claim 1 is objected to because of the following informalities: Claim 1 recites "in photoelectric converter and the first transistor being adjacent to each other in the row direction" in lines 3-4 on page 3 which should be corrected to reads as - **wherein** the photoelectric converter and the first transistor being adjacent to each other in the row direction --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 33 & 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 33 is an improper hybrid claim calling for both an apparatus and the method steps of using the apparatus. Thus, claim 33 is indefinite under 35 U.S.C. 112, second paragraph. See MPEP 2173.05(p). Claim 36 is also rejected as being dependent from claim 33.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 33 & 36 are rejected under 35 U.S.C. 101 because the claimed invention is directed to neither a "process" nor a "machine," but rather embraces or overlaps two different statutory classes of invention. See MPEP 2173.05(p).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 33 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Koizumi (US 7,081,607).

Regarding claims 33, Koizumi discloses an image reading method for a solid-state image sensor (Figs. 18-20) comprising:

a plurality of pixel units (pixels 1 shown in Fig. 20 and details shown in Fig. 18) arranged in a row direction and a column direction, each of the plurality of pixel units including a photoelectric converter (photodiode 3), a first transistor (Q1) for transferring a signal generated by the photoelectric converter, a second transistor (Q3) for amplifying the signal, a third transistor (Q2) for resetting an input terminal of the second transistor, and a fourth transistor (Q4) for reading the signal outputted by the second transistor; a plurality of first signal lines (signal lines 67) extended in the row direction, each of the first signal lines being connected to gate electrodes of the first transistors (Q1) of the pixel units arranged in the row direction (see col. 10, lines 49-61 and col. 12,

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lines 43-55, it is noted that Fig. 18 is similar to Fig. 12 except for that the reset lines 15 of adjacent rows are coupled to a common line 58 for simultaneously resetting the two rows); and a plurality of second signal lines (also shared signal lines 67) extended in the row direction, each of the second signal lines being connected to gate electrodes of the fourth transistors (Q4) of the pixel units arranged in the row direction, the first signal line (67) connected to the gate electrodes of the first transistors (Q1) of the pixel units of an n^{th} row (which is $n-1^{\text{th}}$ row in Fig. 18), and the second signal line (67) connected to the gate electrodes of the fourth transistors (Q4) of the pixel units of an $n+1^{\text{th}}$ row (which is n^{th} row in Fig. 18) being formed of a **common signal line** (common line 67; see col. 10, lines 49-61 and col. 12, lines 43-55), the method comprising the steps of:

simultaneously resetting (by pulsing $\emptyset VR$ on line 58 as shown in Figs. 18 & 19) the photoelectric converters and the second transistors in all the rows (see col. 12, lines 59-63, wherein "all the rows" are considered as *at least* the $n-1^{\text{th}}$ row and n^{th} row as shown in Fig. 18, not necessarily all rows of the image sensor);

after a period of a photo detection time (an accumulation period), simultaneously transferring charges from the photoelectric converters (photodiodes 3) to the gate terminals of the second transistors (Q3) via the first transistors (Q1) in all the rows (see Figs. 18 & 19 and col. 12, line 64 – col. 13, line 34, wherein charges in both rows are transferred simultaneously from the photodiodes 3 by pulsing $\emptyset S2$ and $\emptyset S3$ at the same time as shown in Fig. 19);

reading signals and reading reset voltages in each of the rows (col. 12, line 64 – col. 13, line 34).

Regarding claim 36, as shown in the timing chart of Fig. 19 of Koizumi, the step of resetting the photoelectric converter and the second transistors (indicated by active high of ØVR in Fig. 19) and the step of transferring charges (indicated by active high of ØS2 & ØS3 in Fig. 19) to the gate terminals of the second transistors are performed with signal read lines shut off from peripheral circuits (indicated by active low of Ø22 and Ø24 of peripheral circuits; it is noted that details of peripheral circuits are shown in Fig. 4; see col. 12, lines 64 – col. 13, line 34).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1, 28 & 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi (US 7,081,607 B1) in view of Guidash et al. (US 6,466,266 B1).

Regarding claim 1, Koizumi discloses a solid-state image sensor (Figs. 12 & 14) comprising:

a plurality of pixel units (pixel units 1 shown in Fig. 14 and details shown in Fig. 12) arranged in a row direction and a column direction, each of the plurality of pixel units including a photoelectric converter (photodiode 3), a first transistor (Q1) for transferring

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a signal generated by the photoelectric converter, a second transistor (Q3) for amplifying the signal, a third transistor (Q2) for resetting an input terminal of the second transistor, and a fourth transistor (Q4) for reading the signal outputted by the second transistor (see Fig. 12 and col. 10, lines 49-61);

a plurality of first signal lines (signal lines 67) extended in the row direction, each of the first signal lines being connected to gate electrodes of the first transistors (Q1) of the pixel units arranged in the row direction (see Fig. 12);

a plurality of second signal lines (also shared signal lines 67) extended in the row direction, each of the second signal lines being connected to gate electrodes of the fourth transistors (Q4) of the pixel units arranged in the row direction, the first signal line connected to the gate electrodes of the first transistors of the pixel units of an n^{th} row (which is $n-1^{\text{th}}$ row in Fig. 12), and the second signal line connected to the gate electrodes of the fourth transistors of the pixel units of an $n+1^{\text{th}}$ row (which is n^{th} row in Fig. 12) being formed of **a common signal line** (common line 67) (see col. 10, lines 49-61), and in each pairs of the pixel units of the n^{th} row (which is $n-1^{\text{th}}$ row in Fig. 12) and the $n+1^{\text{th}}$ row (which is n^{th} row in Fig. 12) corresponding to each other, the gate electrode of the first transistor (Q1($n-1$)) of the pixel unit of the n^{th} row and the gate electrode of the fourth transistor (Q4(n)) of the pixel unit of $n+1^{\text{th}}$ row are being formed by one continuous pattern of a conducting material (see Fig. 12).

Although Koizumi teaches the common signal line (67) as a continuous conducting material which is connected to the gate of transistor Q1($n-1$) and the gate of transistor Q4(n) as shown in Fig. 12, Koizumi does not fairly teach that the continuous

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pattern of the conducting material is on a same conducting **layer**, *wherein* [in] photoelectric converter and the first transistor being adjacent to each other in the row direction, the second transistor and the third transistor being adjacent to each other in the column direction, the gate electrode of the first transistor and the gate electrode of the fourth transistor being extended in the column direction.

Guidash teaches a practice for layout of conducting layers for an image sensor in which a common line (TG BUS 23 shown in Fig. 4) connecting to a gate of a transistor of one row and a gate of another transistor of an adjacent row is continuously formed within a same conducting layer (see Guidash, Fig. 4; col. 3, lines 49-65 and col. 4, lines 30-33). Guidash also teaches that photoelectric converter (photodiode 24) and the first transistor (21) being adjacent to each other in the row direction (Fig. 4 shows the *extended portion* of the photodiode 24 located on the right side of the transistor 21 is adjacent to the transistor 21), the second transistor (amplifier 29) and the third transistor (reset transistor 26) being adjacent to each other in the column direction (see Fig. 4), the gate electrode (21) of the first transistor and the gate electrode (RSG) of the fourth transistor being extended in the column direction (see Fig. 4).

Guidash teaches that such layout structure reduces a total of number of signal lines and line contact areas in each pixel, thereby improving fill factor and sensitivity of the image sensor (Guidash, col. 1, line 65 – col. 2, line 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Koizumi and Guidash to arrive at the Applicant's claimed invention so as to reduce a total of number of signal lines and

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line contact areas in each pixel, thereby improving fill factor and sensitivity of the image sensor as taught by Guidash above.

Regarding claim 28, Koizumi in view of Guidash also discloses a contact hole (contact hole at FD shown in Fig. 4 of Guidash) opened onto a source region of the third transistor (which is the source of the reset transistor RG) is formed by self-alignment (i.e., in column direction) with the gate electrode (reset gate 26) of the third transistor (see Guidash, Fig. 4).

Regarding claim 39, Koizumi in view of Guidash also discloses a contact hole opened onto a source region of the fourth transistor (source hole of RSG transistor in Fig. 4 of Guidash) is formed by self-alignment (i.e., in a row direction) with the gate electrode of the fourth transistor (see Fig. 4 of Guidash).

Allowable Subject Matter

7. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
8. Claim 40 is allowed.

The following is a statement of reasons for the indication of allowable subject matter:

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Regarding claims 2 & 40, the prior art of record fails to teach or fairly suggest the limitations required in each of claims 2 & 40 including **“...the common signal lines of the first signal lines and the second signal lines being formed of a first metal interconnection layer, the third signal lines being formed of a second metal interconnection layer, the fourth signal lines and the fifth signal lines being formed of a third metal interconnection layer.”**

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A handwritten signature in black ink, appearing to read 'Nhan T. Tran', with a long horizontal flourish extending to the right.

NHAN T. TRAN
Patent Examiner